# Parallelization of IIR filters in the DFT domain

Christoph Dalpiaz

University of Applied Sciences Upper Austria, Hagenberg

April 1, 2022

UNIVERSITY OF APPLIED SCIENCES UPPER AUSTRIA
OBERÖSTERREICH

Interreg
Austria-Czech Republic
European Regional Development Fund
EUROPEAN UNION

CADSP

# First order IIR filter

$$Y(z) = H(z) \cdot X(z) \qquad H(z) = \frac{1}{1 + a \cdot z^{-1}}$$

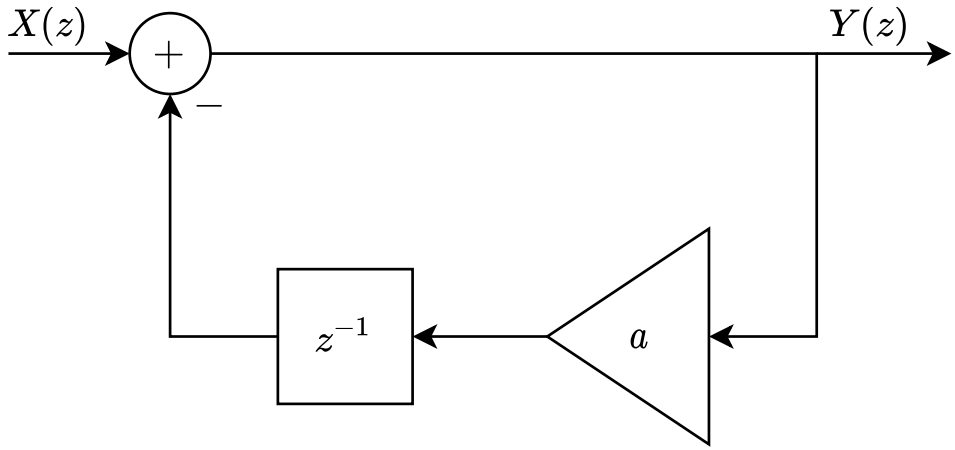


Figure 1: First order IIR filter

- Critical path : One multiplication plus one addition
- Objective : Parallel implementation in order to increase the sampling frequency by a factor of M

# Clock signals

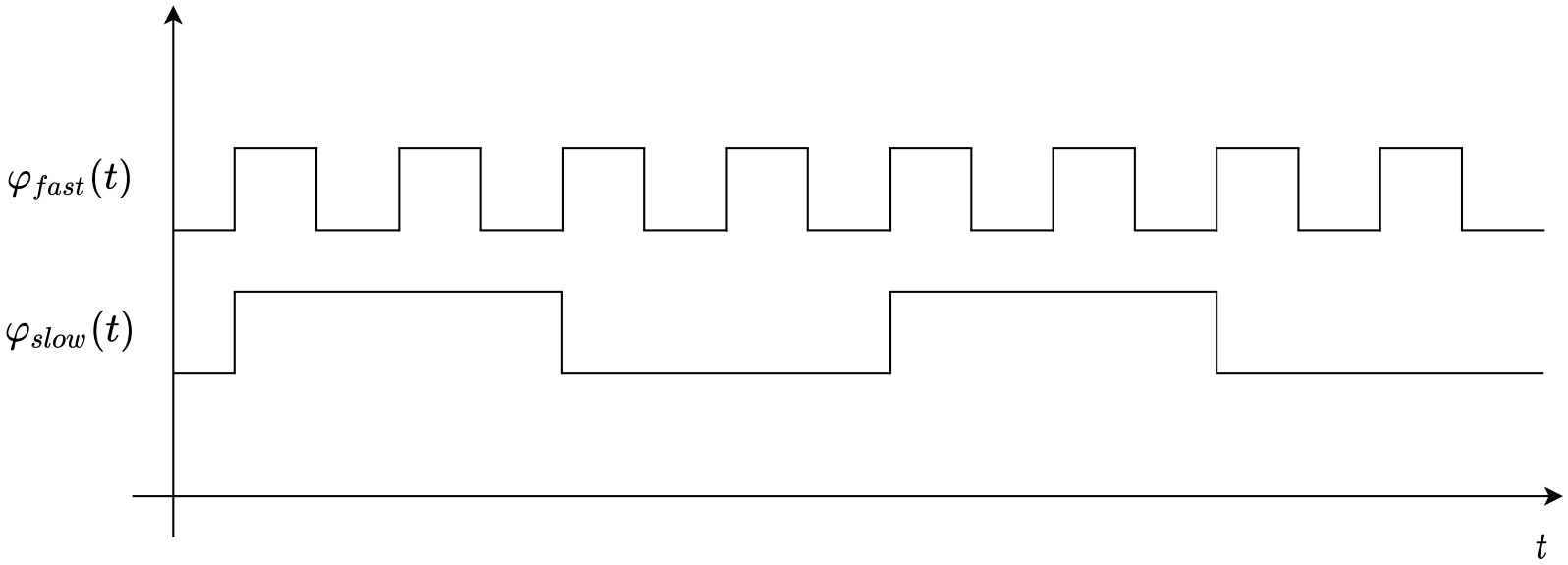


Figure 2: Clock signals of Multirate-System for a parallelization factor $M = 4$

# Multirate-System architecture

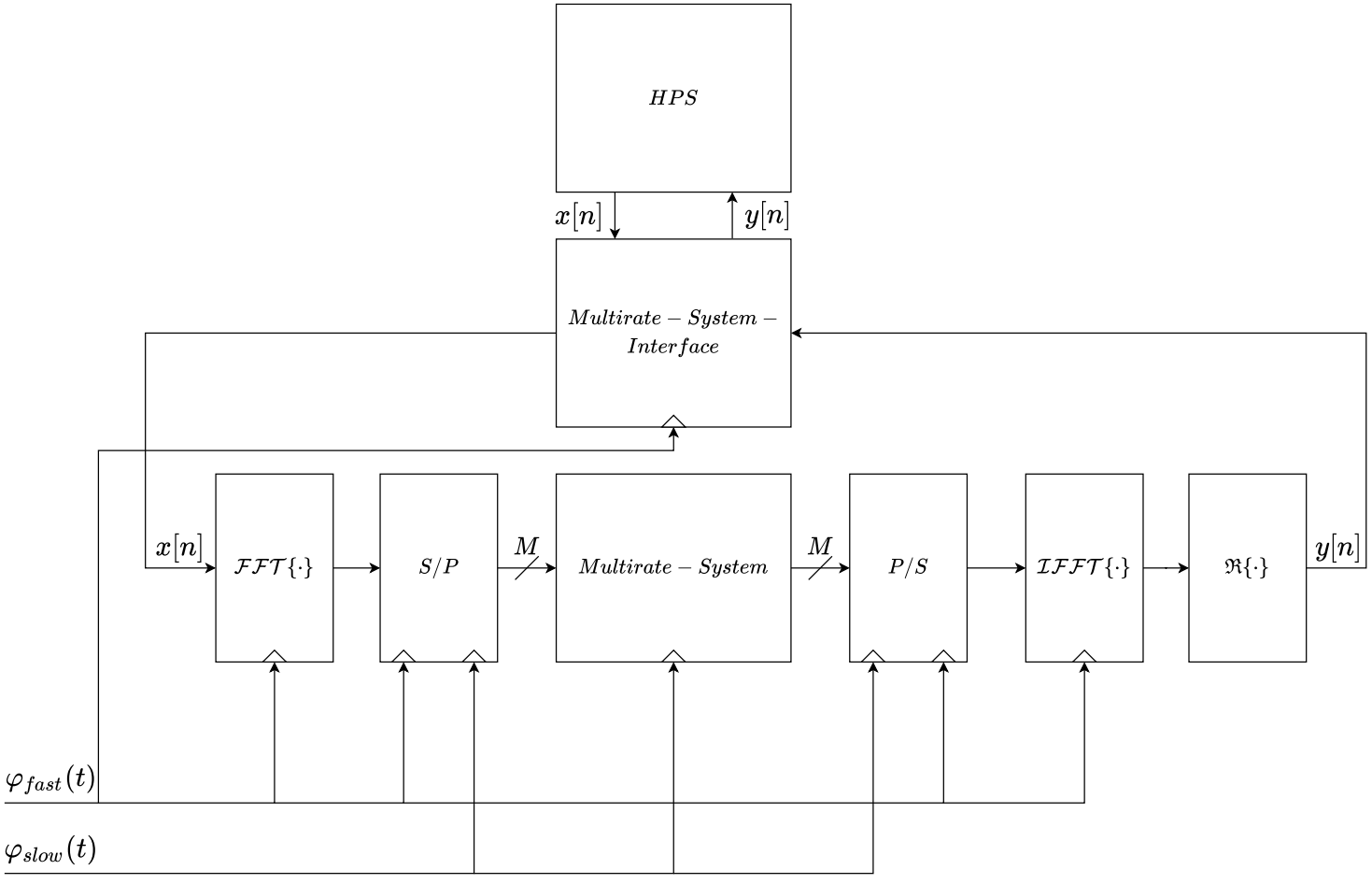


Figure 3: Architecture of Multirate-System implementation

# Pole-zero plot of test filter

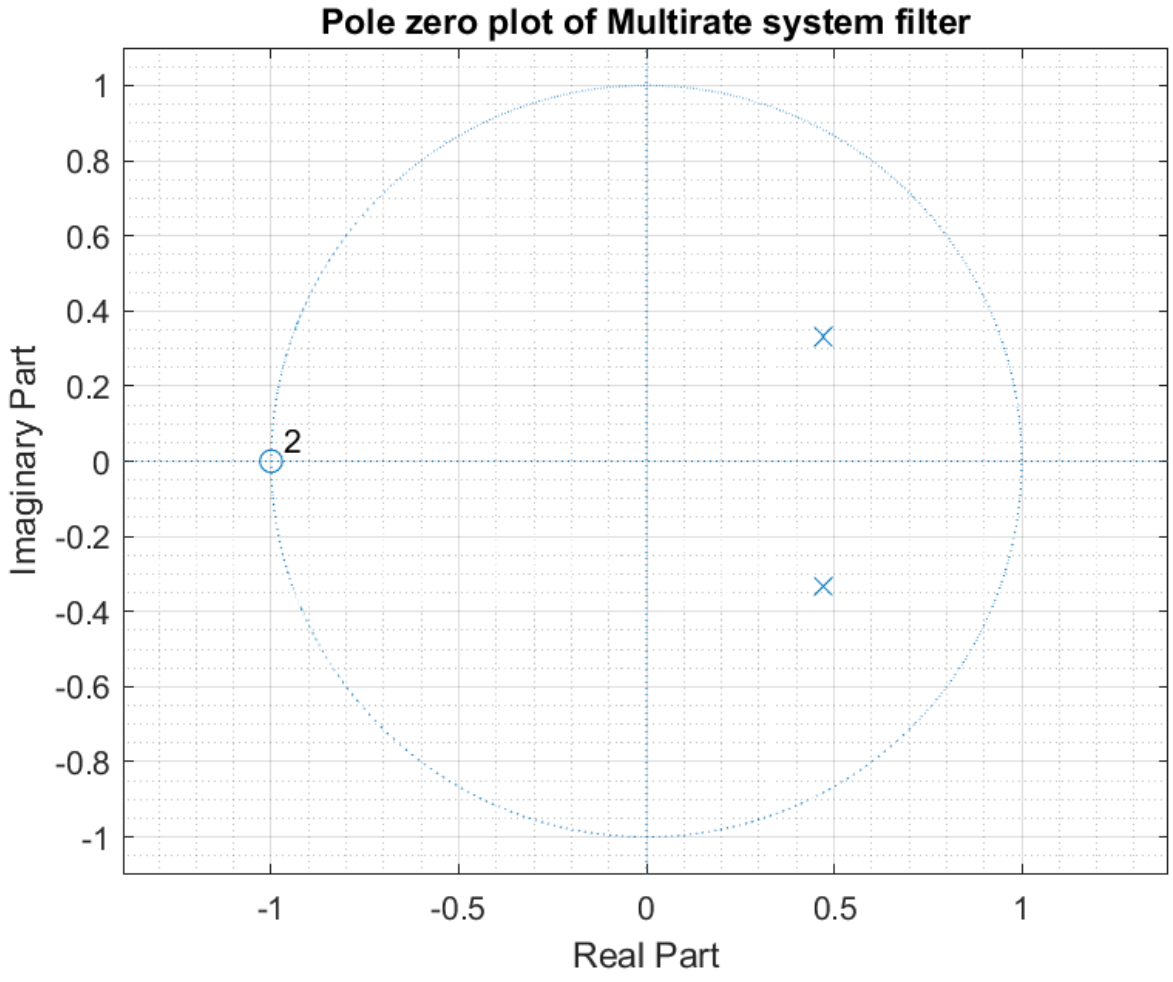


Figure 4: Pole-zero plot of $2^{nd}$ order Butterworth filter

# Input signal of Multirate-System

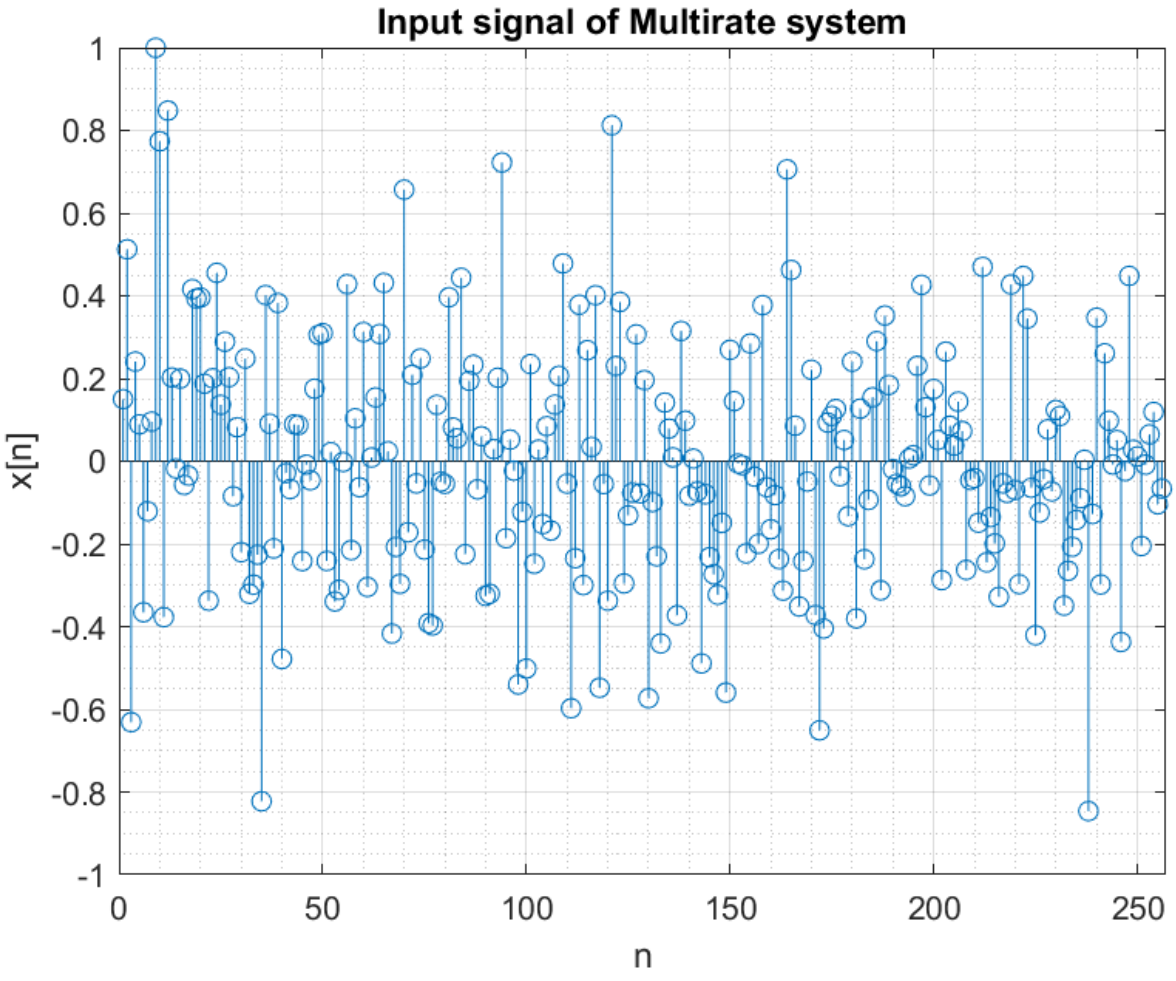


Figure 5: Normally distributed random numbers, 4 blocks of length 64

# Output signal of Multirate-System

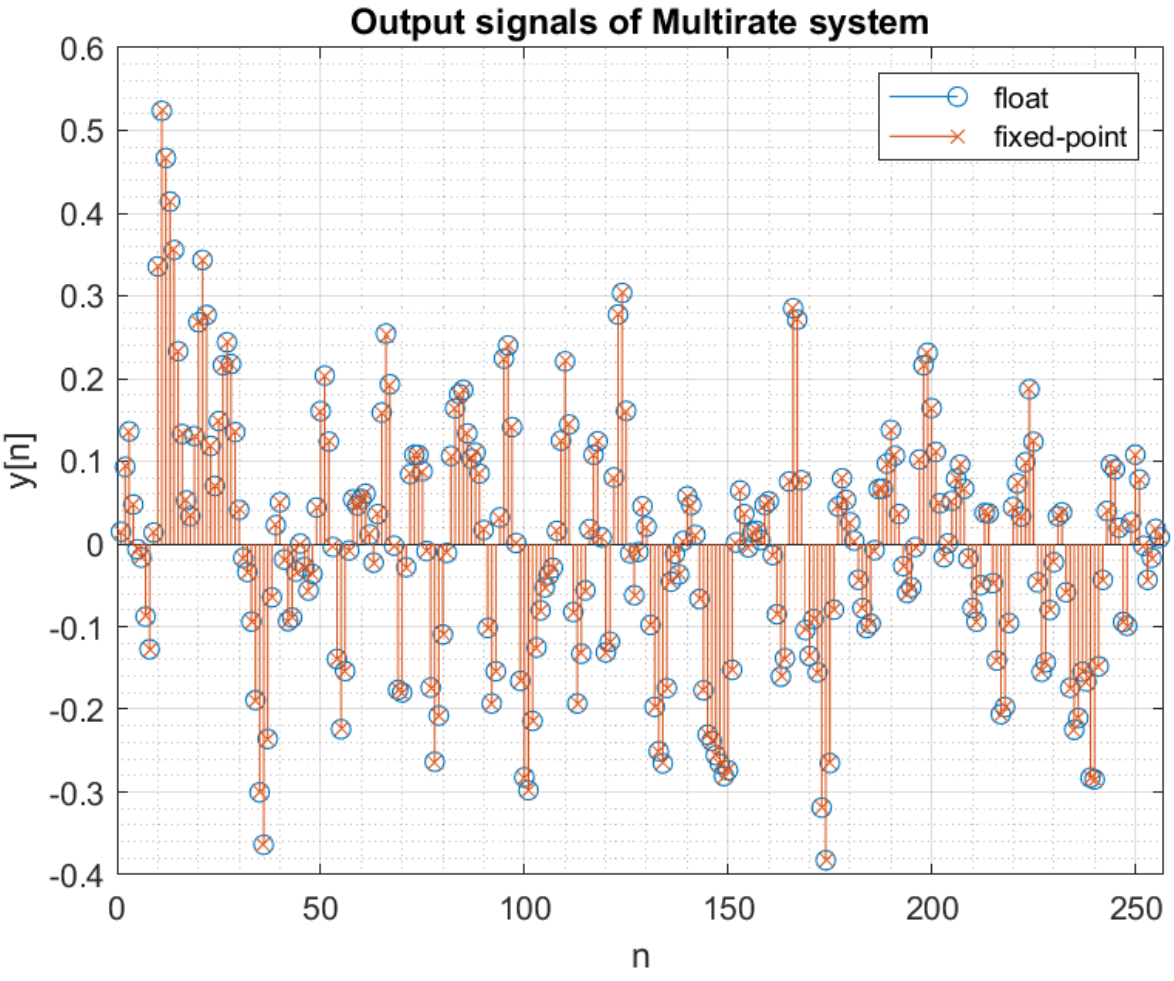


Figure 6: Output signal, float and 6.12 fixed-point

# Output signal deviations

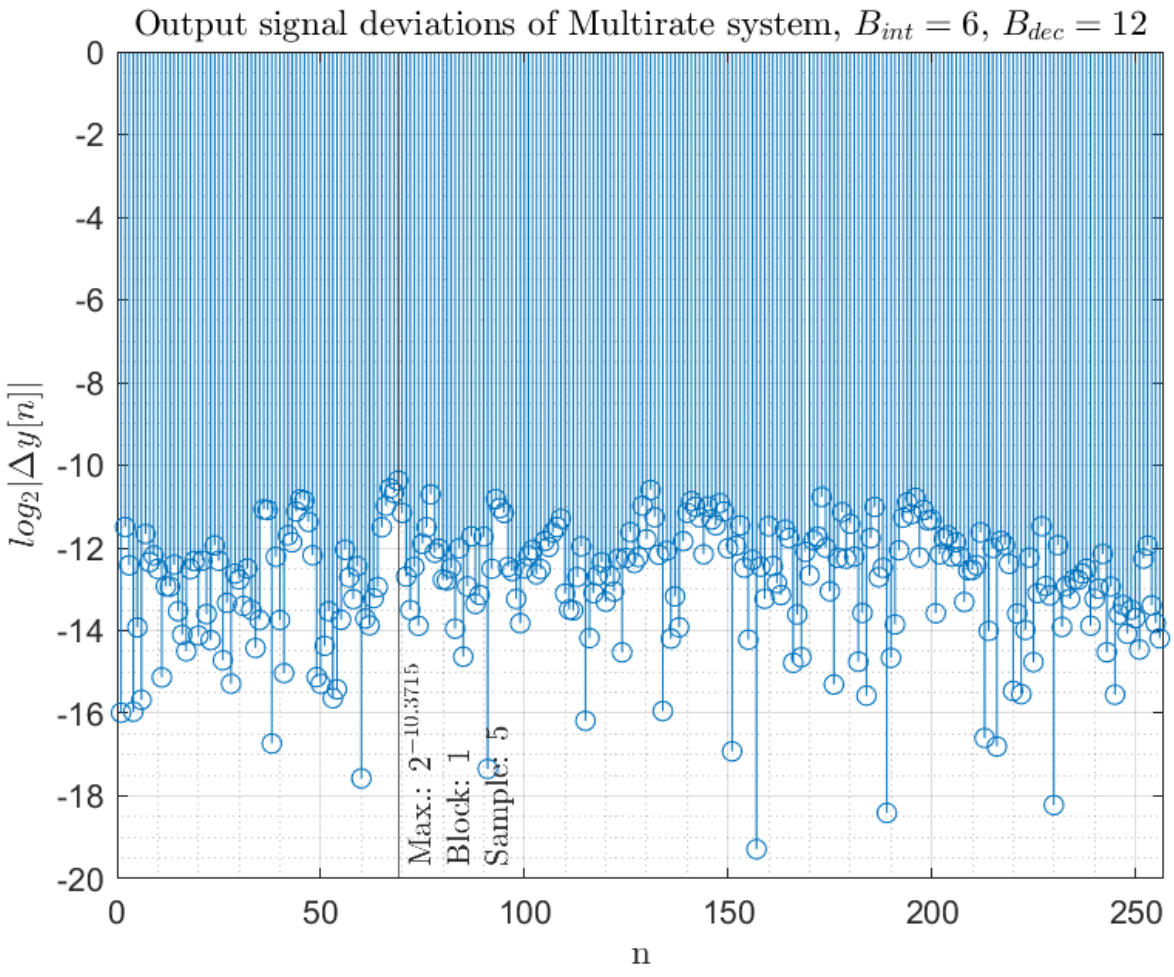


Figure 7: Deviations between float and fixed-point implementation

# Synthesis result for Intel Cyclone V FPGA

Configuration:

- $M = 2$
- $Integer\ bitwidth = 6$
- $Decimal\ bitwidth = 12$

Performance :

- $\varphi_{slow,max} \approx 32\ MHz$
- $\varphi_{fast,max} \approx 84\ MHz$

Complexity:

| Resource | Complete design | FFT and IFFT |
|---|---|---|
| ALMs | $\frac{5914}{32070} \approx 18.4\%$ | $\frac{4263}{32070} \approx 13.3\%$ |
| M10K blocks | $\frac{53}{397} \approx 13.4\%$ | $\frac{48}{397} \approx 12.1\%$ |
| DSP blocks | $\frac{58}{87} \approx 66.7\%$ | $\frac{12}{87} \approx 13.8\%$ |