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RFSoC for data generation and acquisition

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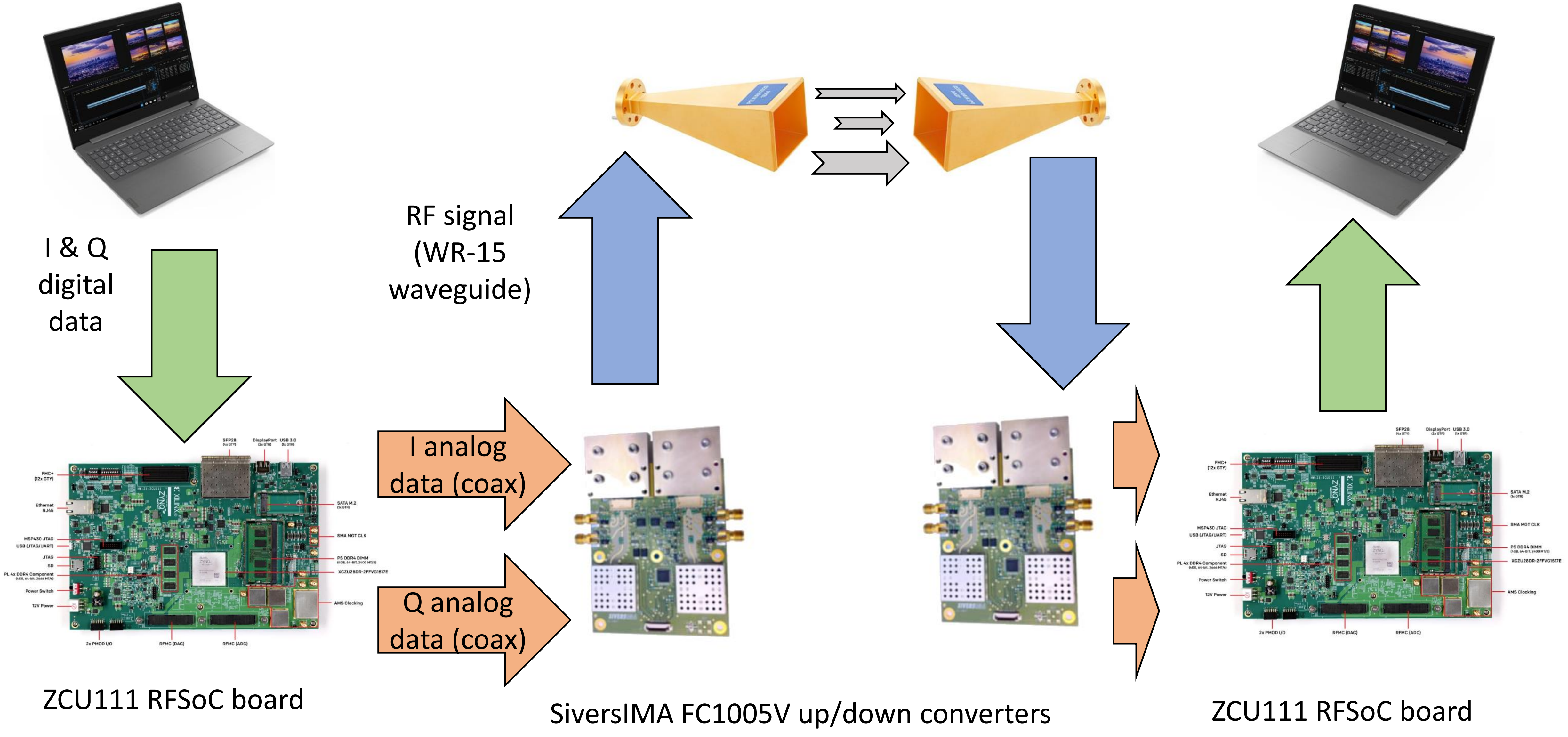
Example: 60 GHz measurement setup



I & Q digital data

RF signal (WR-15 waveguide)

I analog data (coax)

Q analog data (coax)

ZCU111 RFSoC board

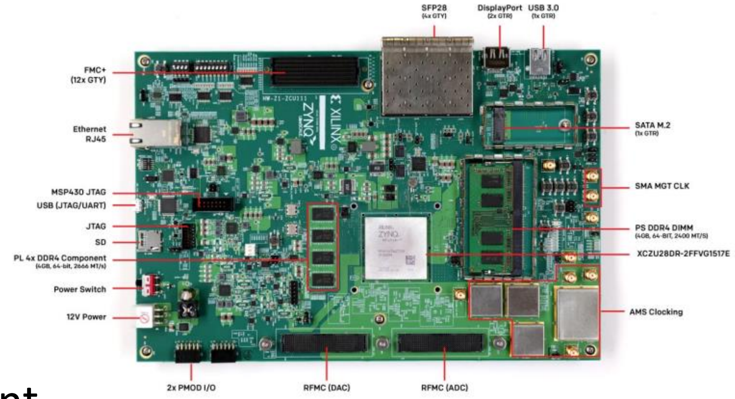
SiversIMA FC1005V up/down converters

ZCU111 RFSoC board

TX side: useful signal bandwidth 512 MHz

Throughput at this point is not important, used only for loading arbitrary (OFDM, OTFS…) signal into RFSoC memory, which then repeats seamlessly.

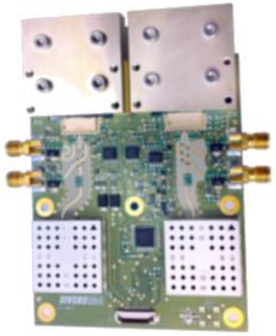
2048 MSPS -> 2x interpolation -> DACs @ 4096 MHz



ZCU111 RFSoC board

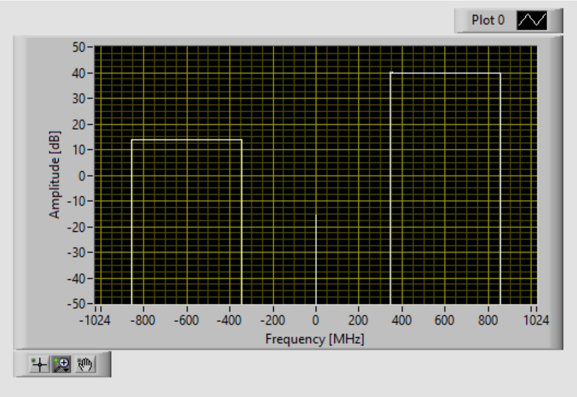
I analog data (coax)

Q analog data (coax)



SiversIMA FC1005V up/down converter
10 MHz – 4 GHz IF
I and Q analog inputs to mixer

To compensate the SiversIMA‘s I/Q imbalance, the signal is 4x interpolated and digitally (on PC) shifted to carrier frequency of 600 MHz and inverse I/Q imbalance is introduced. The resulting complex signal has sampling frequency of 2048 MSPS.



Substantial I/Q imbalance

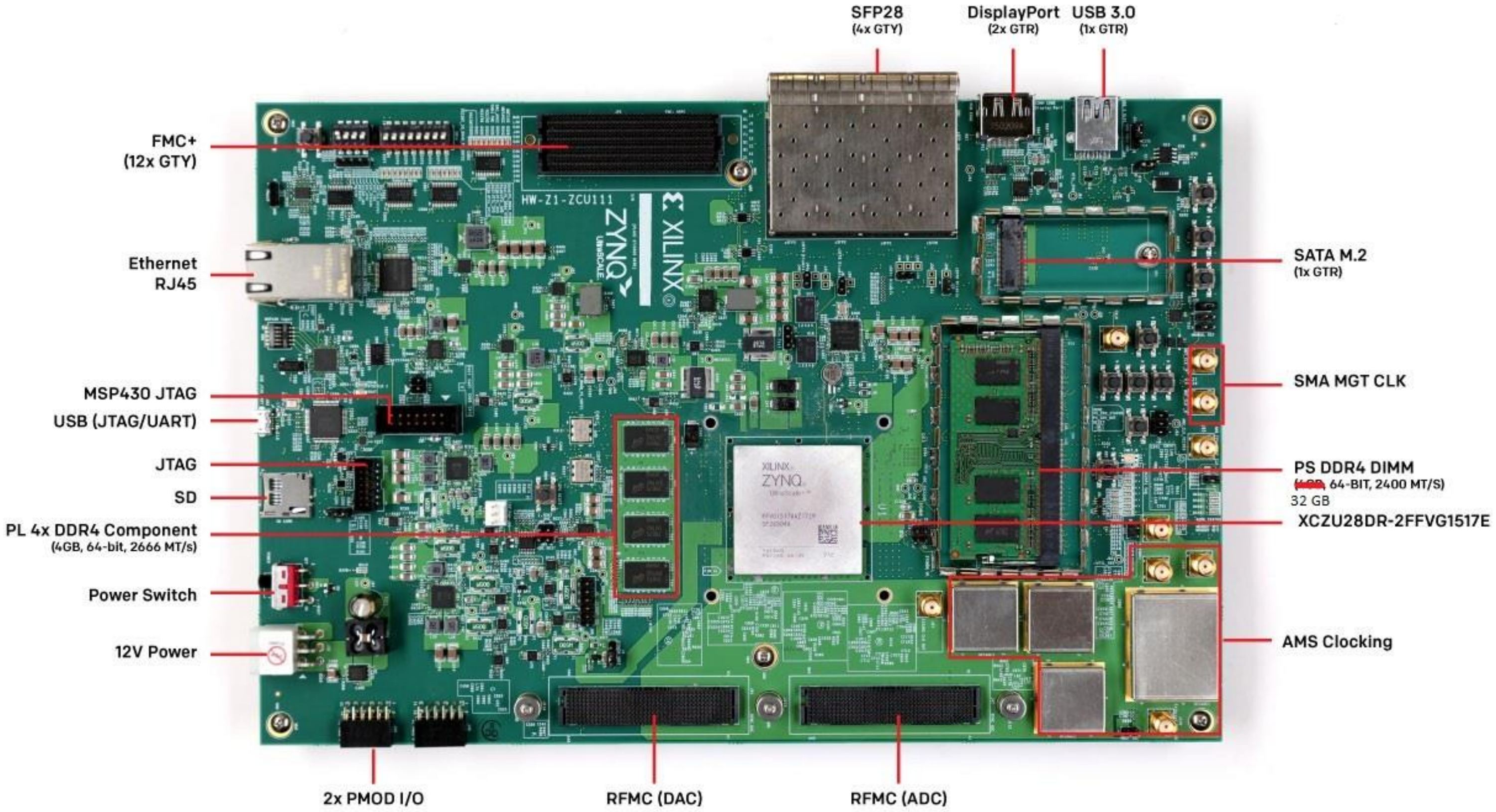
TX side

Data format: i16 for real part, i16 for imaginary part of the signal = 4 bytes per sample.

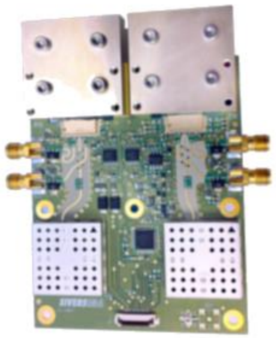
Default (current) settings:
128 MiB per channel from PL DDR = 32 MS
= 0.0625 s @ 512 MSPS
= 0.015625 @ 2048 MSPS

Could be changed easily (up) to:
4 GiB for one channel from PL DDR = 1024 MS
= 2 s @ 512 MSPS
= 0.5 s @ 2048 MSPS

Could also use PS memory (?)



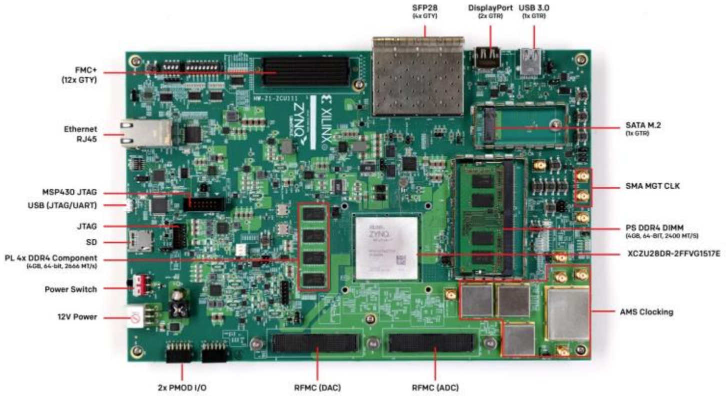
RX side: useful signal bandwidth 512 MHz



I analog data (coax)

Q analog data (coax)

ADCs @ 4096 MSPS -> digital mixing -> 8x decimation -> 512 MSPS



ZCU111 RFSoC board

Throughput at this point is not important, used only for offloading data from RFSoC memory.

SiversIMA FC1005V up/down converter
10 MHz – 4 GHz IF
I and Q analog outputs from mixer

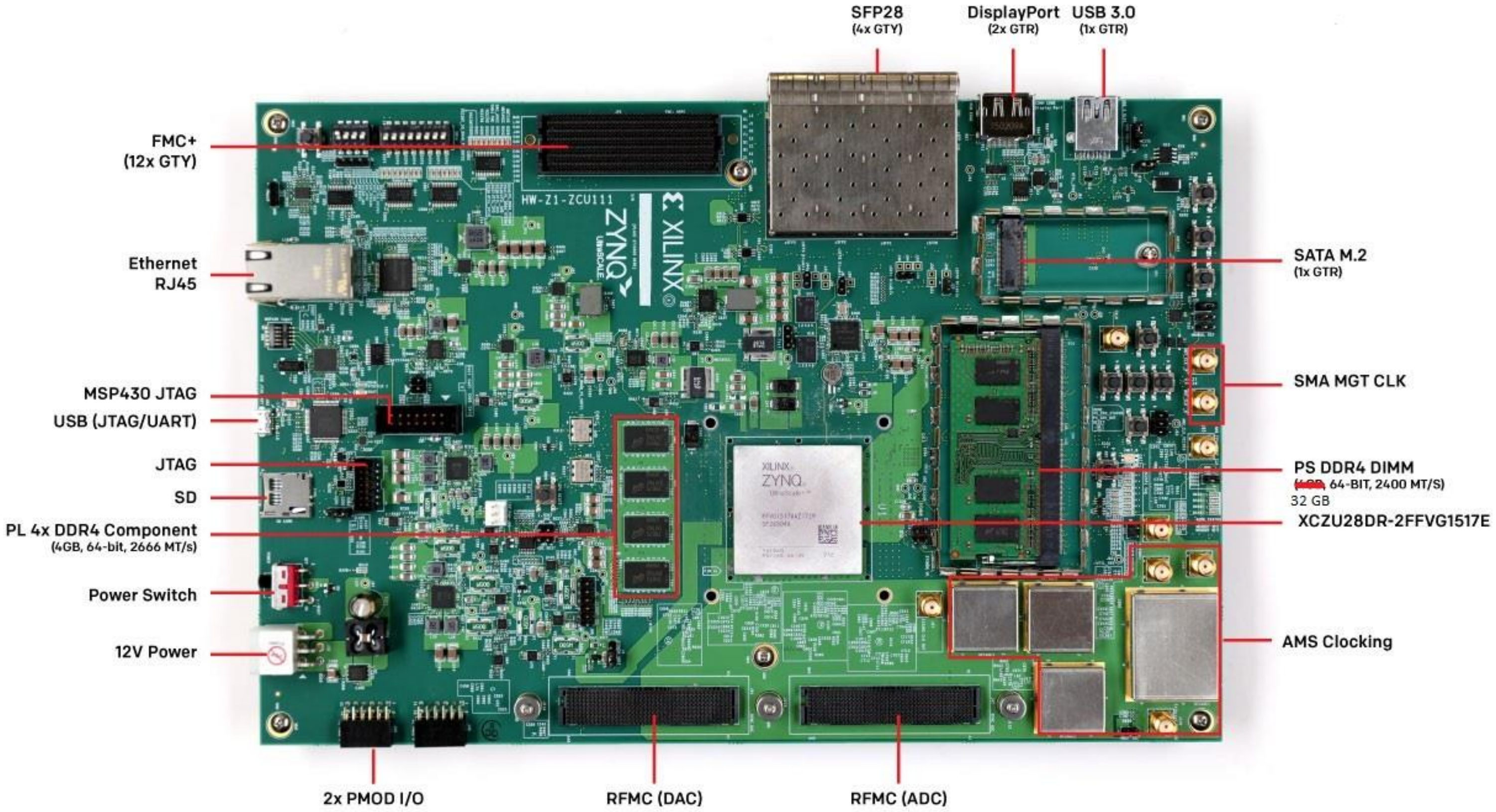
RX side

Data format: i16 for real part, i16 for imaginary part of the signal = 4 bytes per sample.

Default settings:
128 MiB per channel from PL DDR = 32 MS
= 0.0625 s @ 512 MSPS
= 0.015625 @ 2048 MSPS

Current settings:
28 GiB for one channel from PS DDR = 7 GS
= 14 s @ 512 MSPS
= 7 s @ 1024 MSPS

The recorded stream also does not have to be continuous – it is possible to e.g. record 1000 samples, then discard 20000 samples, record another 1000 and so on – implemented in FPGA.

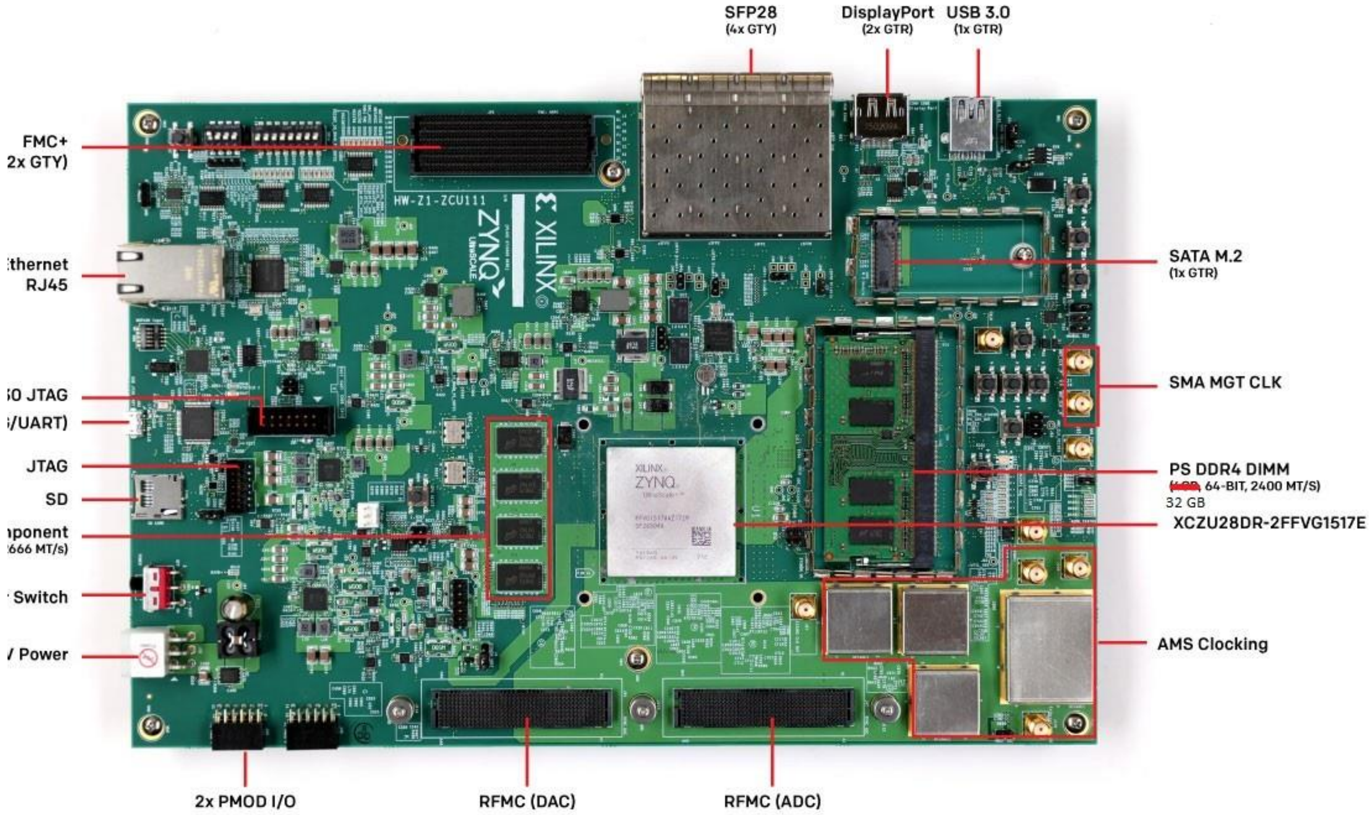


PS memory upgrade

PL memory – hard soldered DDR4 chips.
PS memory – 4 GB DDR4 module -> changed to 32 GB

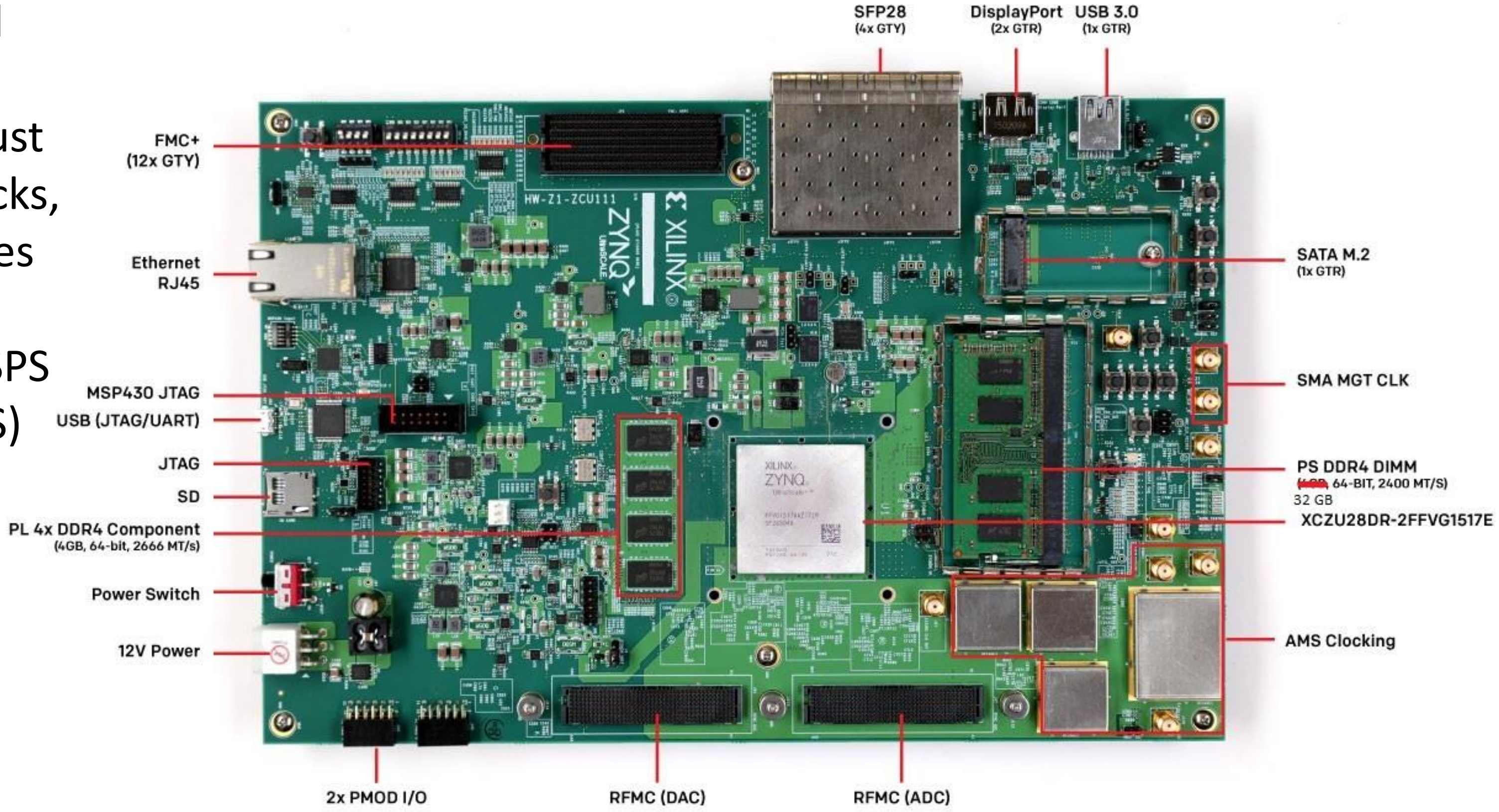
Lot of tweaking and experimenting:

- Vivado design changes, export hardware to Petalinux
- Changes in system device tree
- Change & recompile linux kernel (memory page size) for allocating huge continuous blocks of memory
- Improvements in the kernel memory driver (i32 size variables = 2 GiB limit, u32 = 4 GiB -> u64)
- Improvements in the linux server application (also variable size issues; send large chunks of data over TCP to PC client)



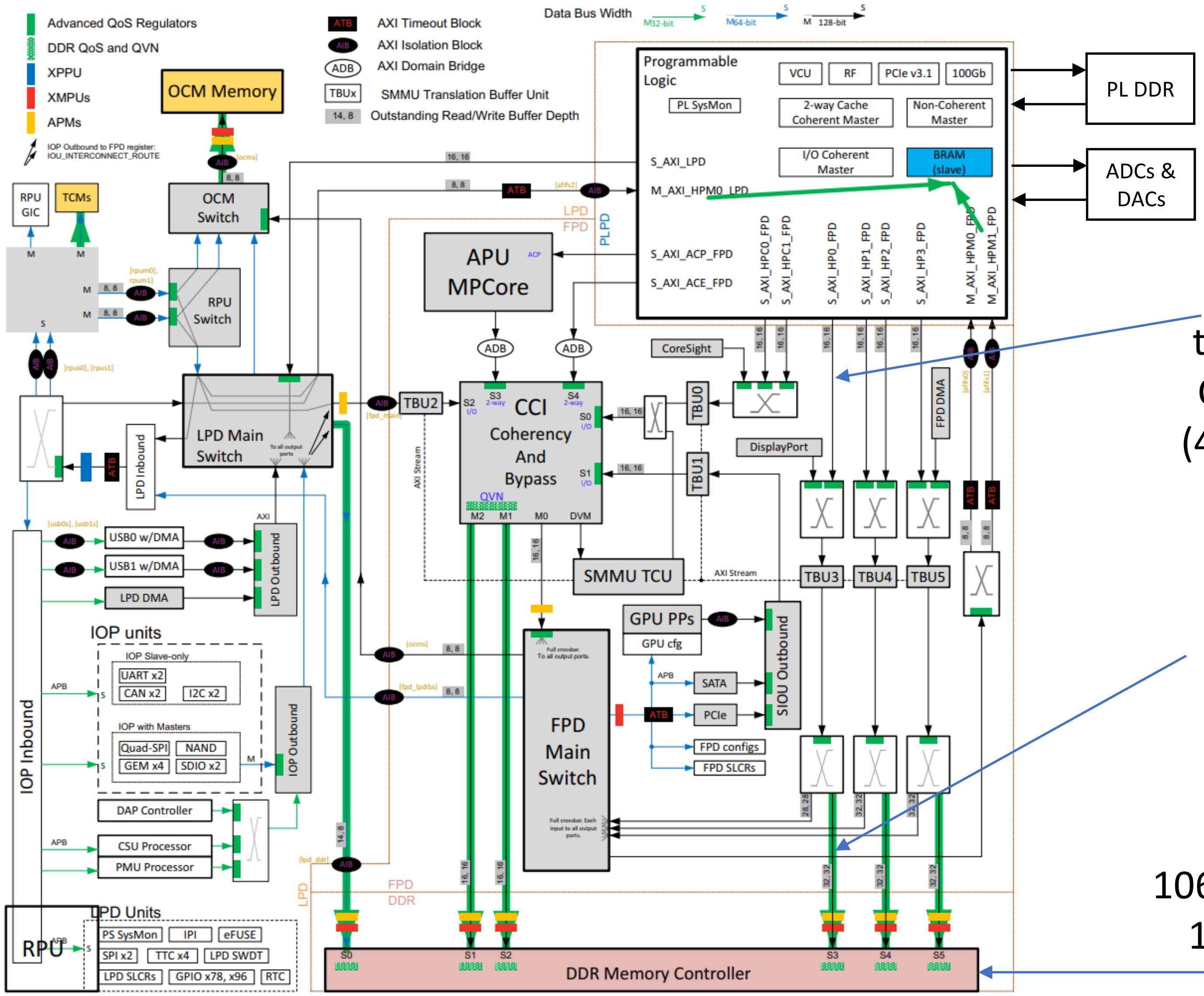
Throughput bottlenecks

2666 MT/s * 64b/8 =
21.3 GBPS theoretical throughput
9.5 GBPS measured, must investigate further – clocks, FPGA design, (AXI) buses width…
Still capable of 2048 MSPS streaming (8096 MBPS)



2400 MT/s * 64b/8 =
19.2 GBPS theoretical throughput

PS memory throughput bottleneck



300 MHz * 128b/8 =
4.8 GBPS theoretical
throughput per HP port
Can handle 1024 MSPS
(4.096 GBPS) throughput

533 MHz * 128b/8 =
8.5 GBPS theoretical
throughput

1067 MHz * 2 * 64b/8 =
17 GBPS theoretical
throughput

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Thank you

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