Implementation of LWDFs and Hilbert-Transformers in VHDL

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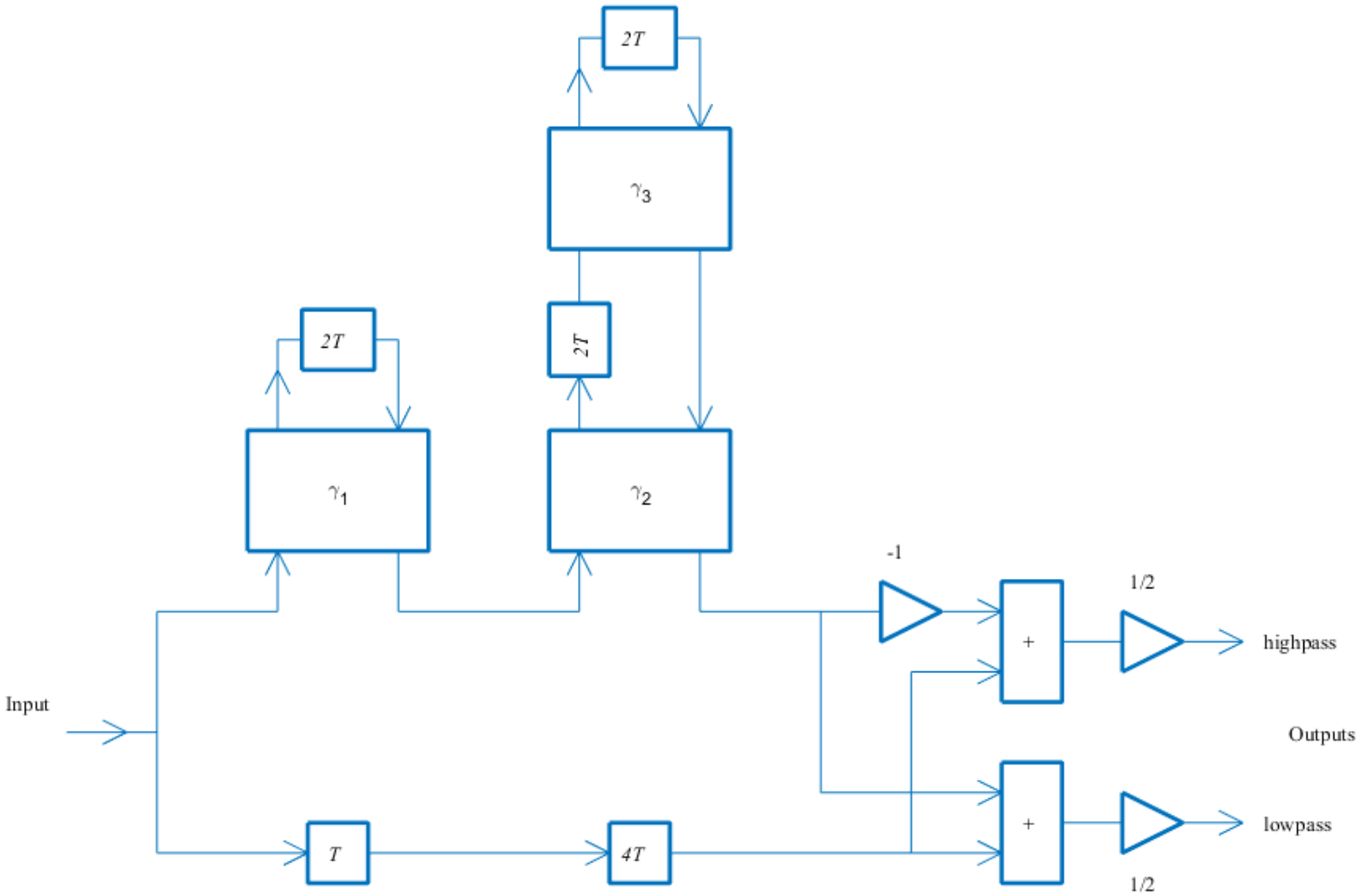
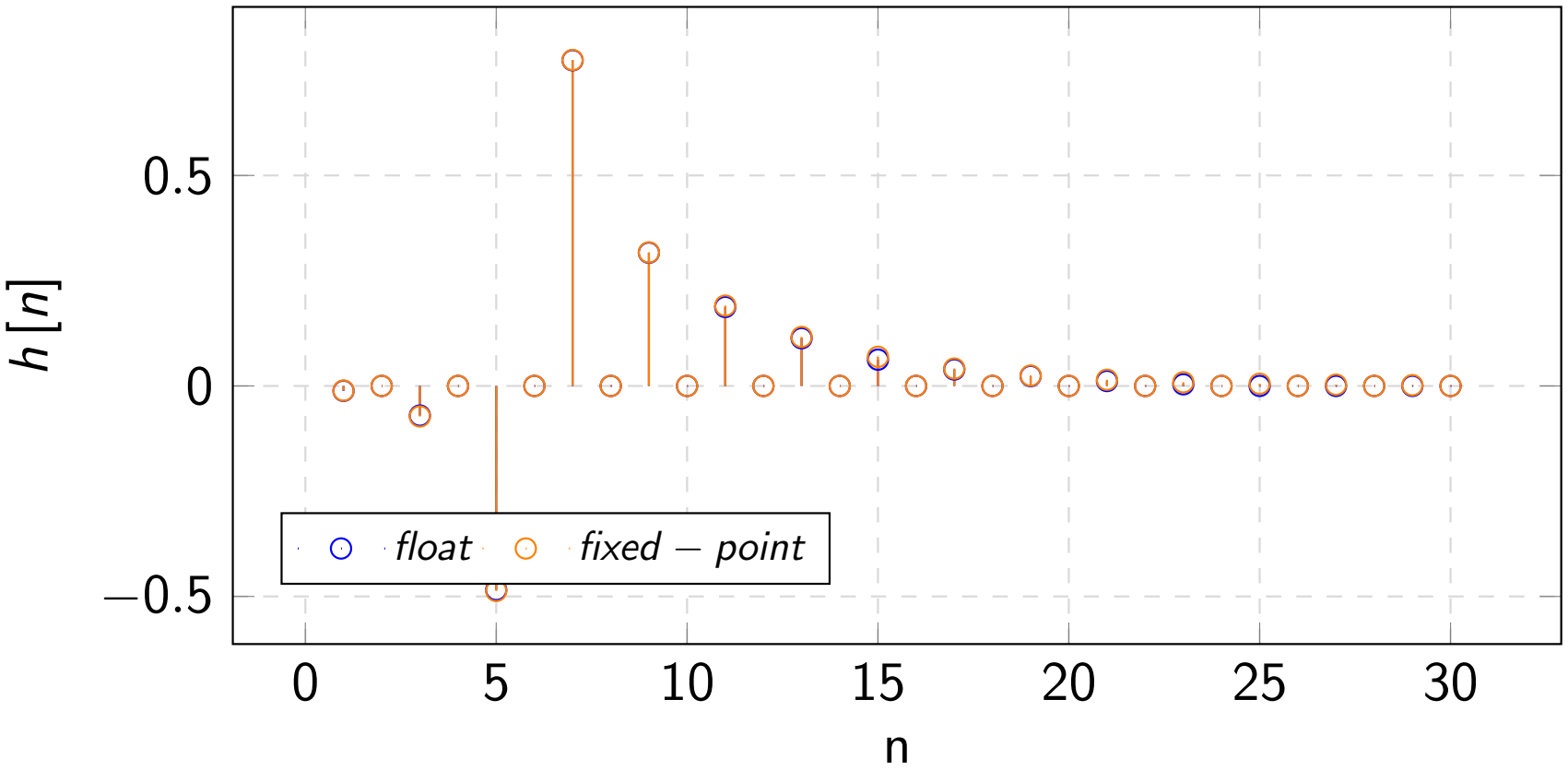
LWDF-Structures



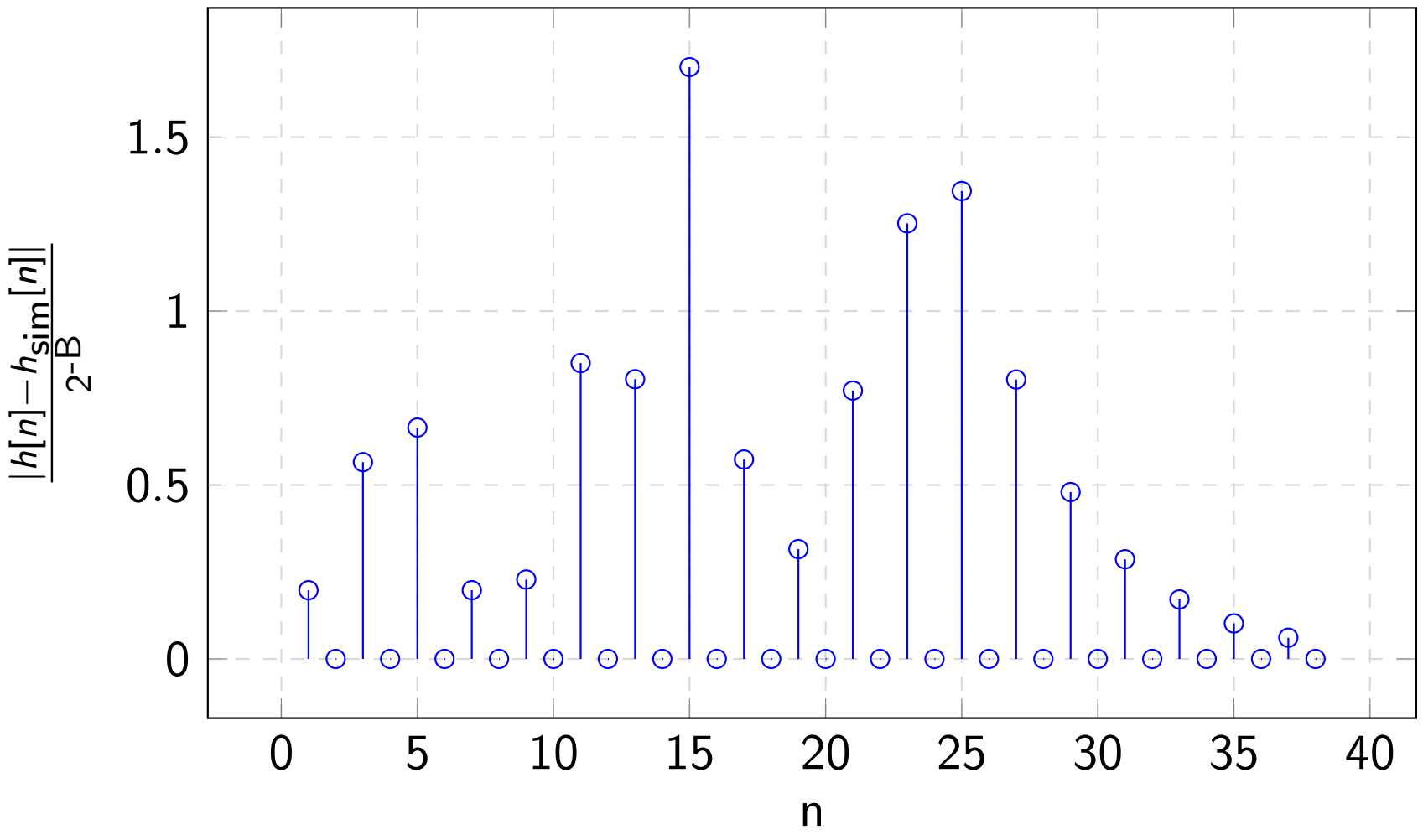
Hilbert-Transformer with order 6 - impulse response



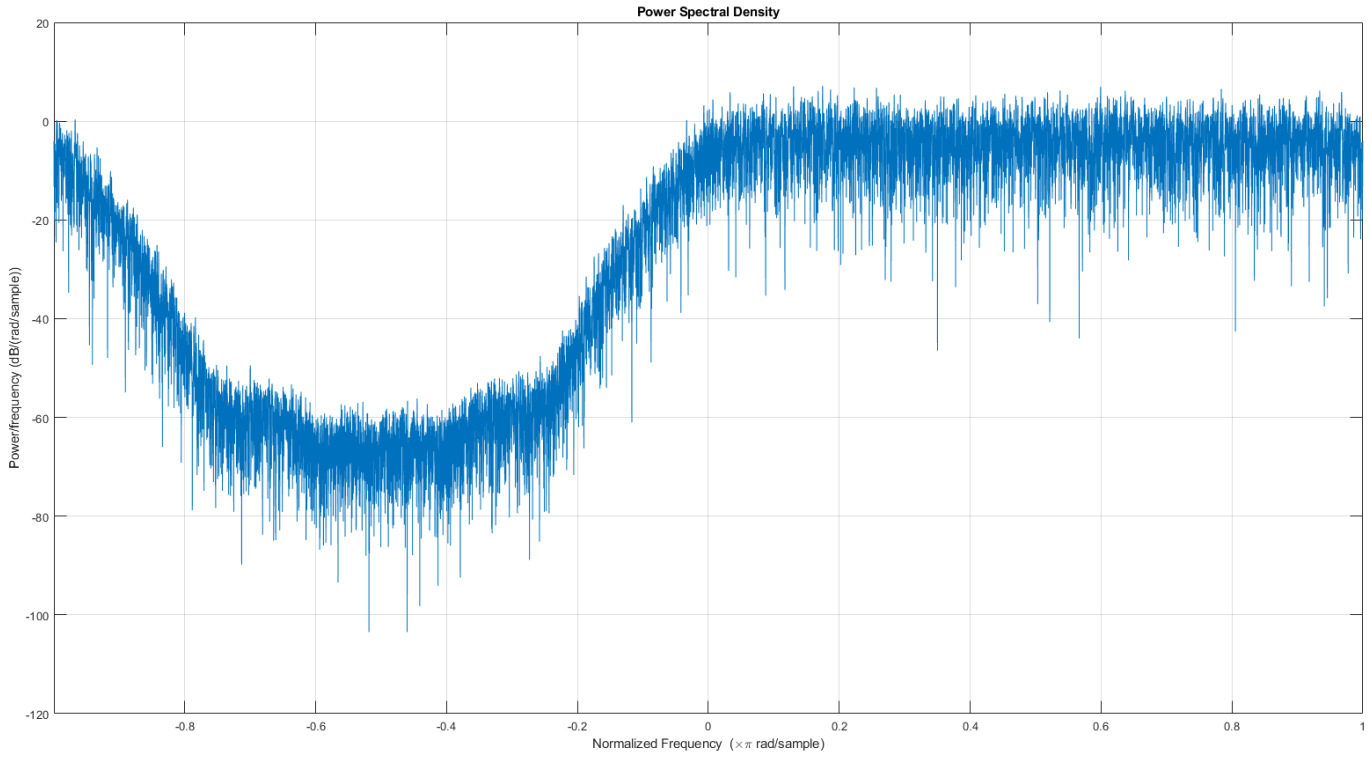
Canonical signed digit representation:

$\gamma = \sum_{i=1}^{B} \gamma_i \cdot 2^{-i}$ $\qquad\qquad$ $\gamma_i \in \{0, \pm 1\}$

Hilbert-Transformer with order 6 - absolute deviations in impulse response



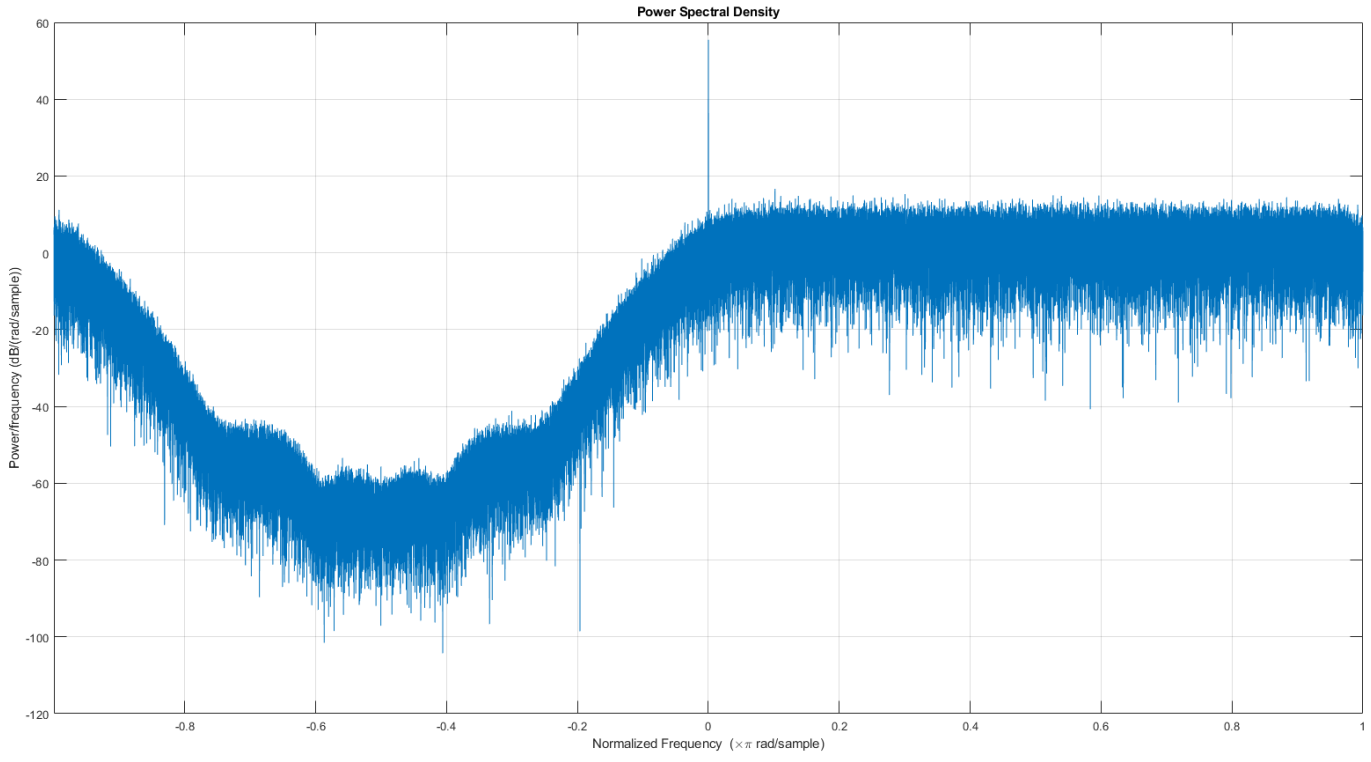
Hilbert-Transformer with order 6 - simulation result



Configuration: Integer bitwidth=5
Decimal bitwidth=8
Internal decimal bitwidth=10

Test on DE1-SoC (Intel Cyclone V FPGA)

Hardware-Test with Intel FPGA Platform-Based-Design.
Samples have been transmitted to FPGA from ARM Cortex-A9.



Performance and Hardware-Complexity

Performance:	maximum clock frequency ≈ 67.91 MHz
	$f_n \approx 33,96 MHz$
	$B \approx f_n \cdot 60\% \approx 20.38 MHz$
Complexity:	3 coefficients with 3 non-zero digits
	Dash-operations for coefficients $= 9$
	Total number of dash-operations $= 18$