Current State of Development of SDR for InterOP

InterOP – ATCZ175

Interoperabilita heterogenních radiových systémů

SIX Research Centre

Brno University of Technology

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Österreich-Tschechische Republik
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Architecture

- Modular
  - FPGA module: TE0803 with Zynq Ultrascale+
  - RF Frontend: HW compatible with SBX, WBX, … by Ettus Research
- ADC – 250 MSps, **14/16** b
- DAC – 500/1000 MSps, 16 b
- Connectivity: 1G Ethernet, USB for Debugging
- GPIOs, RS-232

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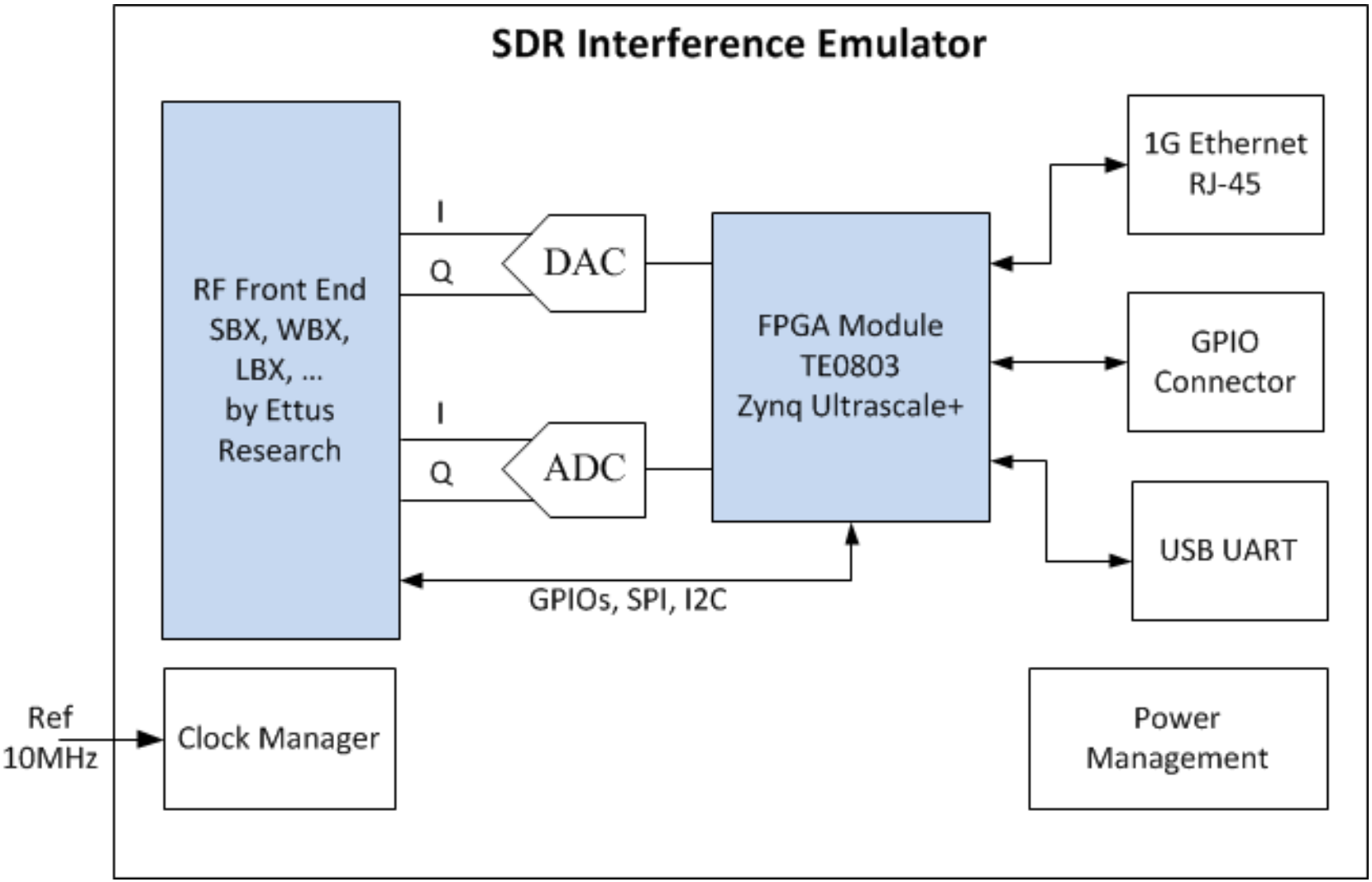
Block Diagram



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Already Done Tasks

- Rx (FPGA to PC) Streaming (Jan K.)
  - High throughput Ethernet communication *bermetal
- ADC and DAC Interfaces (Michal H., Martin P.)
  - Samples acquisition from ADC *w/o proper timing
  - Samples generation for DAC *w/o proper timing
- Embedded Linux (Aleš P., Jan K.)

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Rx / Tx Streaming

- Current state
  - Maximum throughput < 1 Gbps => < 25 MSps @ 16b (2x400Mbps benchmark)
  - Zero-copy => DMAs for Rx/Tx from/to FPGA, DMAs for UDP communications
- Next step
  - Tx side
  - Flow control for Tx Stream
  - Time and Events synchronization (up to 1 sample precision)

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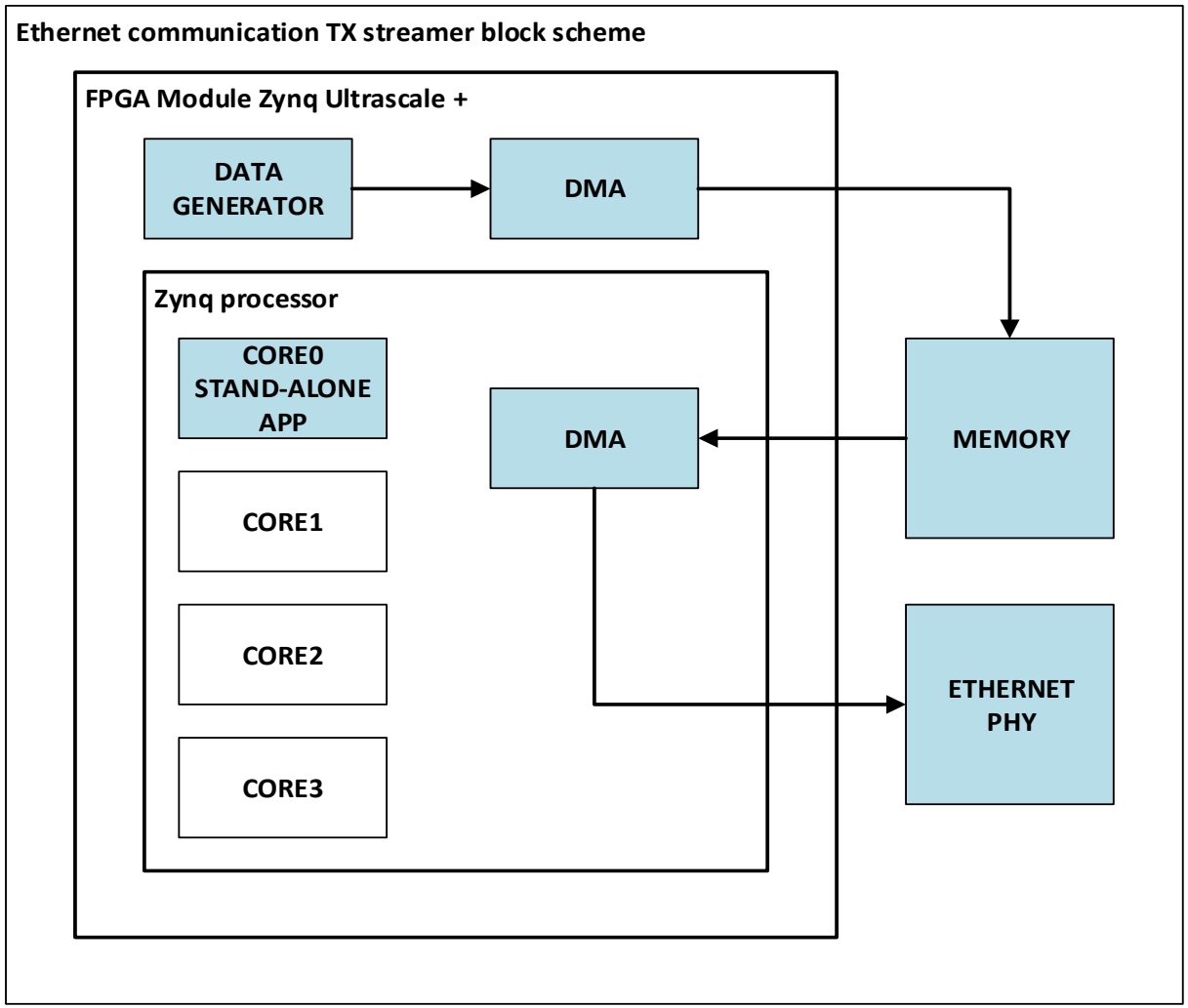
Rx Streaming current state



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ADC and DAC Interfaces

- Current state
  - Block for setting of acquisition clock phase for deterministic delay
  - Implementation of parallel data interfaces (SERDES)
  - Deterministic sample delay for Data pairs (acquisition of de-seralized samples at 125 MHz)
- Next setp
  - Provide timing synchronization of data bus with ADC acquisition clock domain.
  - DAC timing constraints and its compensation

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Embedded Linux

- Motivation
  - Serious limitations for baremetal (no OS) and “small” systems, e.g. FreeRTOS
- Petalinux – Xilinx extension of Yocto Linux
  - Targeted for embedded applications
  - Highly modular / highly optimized
- Current state
  - Implementation Petalinux on ZedBoard and also on TE803 but with Ethernet PHY issues – driver problem
- Plan
  - Benchmarking using Rx / Tx Streaming application on linux

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