Specification of Target Platform for InterOP

InterOP – ATCZ175

Interoperabilita heterogenních radiových systémů

SIX Research Centre

Brno University of Technology

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Architecture

- Modular
  - FPGA module: TE0803 with Zynq Ultrascale+
  - RF Frontend: HW compatible with SBX, WBX, … by Ettus Research
- ADC – 250 MSps, 12/14 b
- DAC – 500/1000 MSps, 16 b
- Connectivity: 1G Ethernet, USB for Debugging
- GPIOs, RS-232

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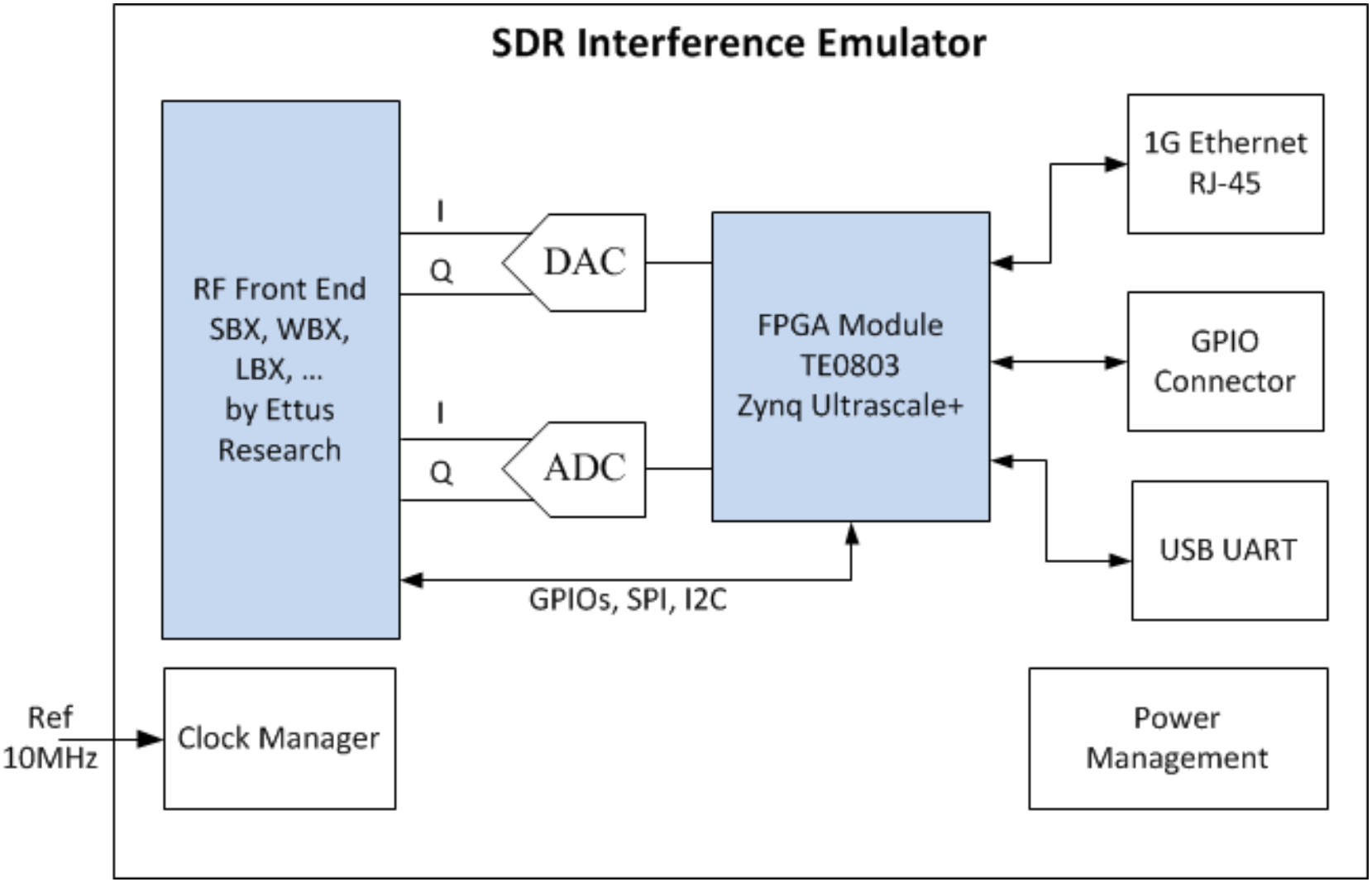
Block Diagram



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Current State

- Specification of SDR concept
- Design of HW - first SDR prototype
- Basic software modules:
  - Ethernet
  - DAC interface
  - ADC interface
  - Initial implementation of Command protocol
  - Data streaming using DMA

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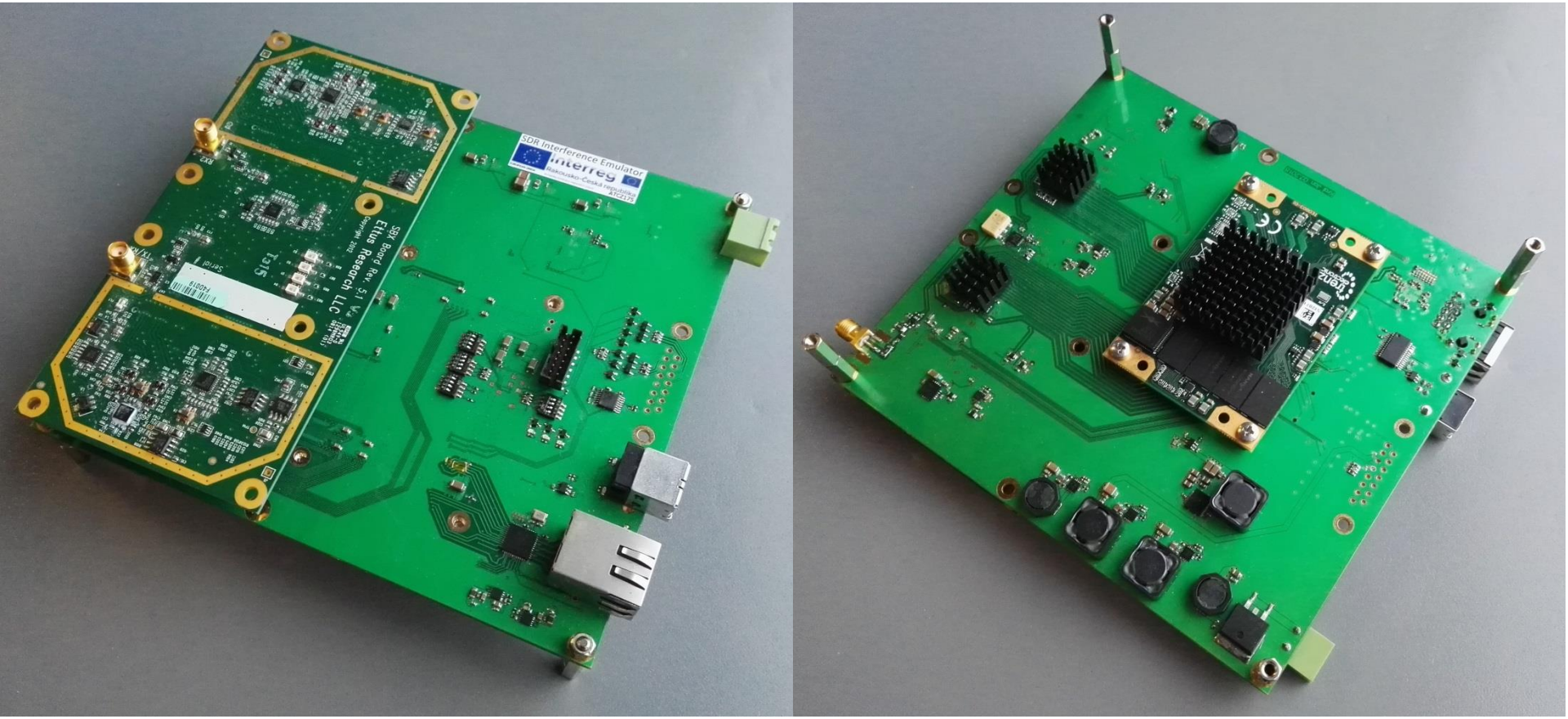
First HW Realisation



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Future Work

- Use cases:
  - Record - Replay
  - …. (discussion)
- New HW revision:
  - SFP (fiber optic), SATA (for SSD), PCI-e (x4), HDMI, … (discussion)

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